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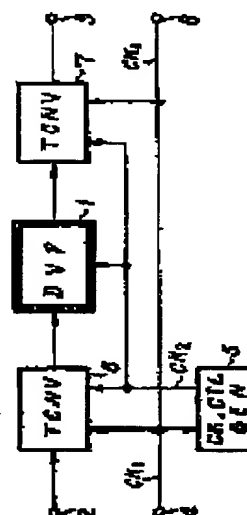
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(54) PROCESSOR OF DIGITAL SIGNAL

(57)Abstract

PURPOSE: To attain the shared use of a signal processor, by constituting a processor of digital signals of different sampling frequencies so that it can process a digital signal having a high sampling frequency and supplying the signals after converting the time axis of the digital signal having a low sampling frequency.
CONSTITUTION: A video data processor 1 is so constituted as to actuate the higher sampling frequency (fsh) than the sampling frequency (fsl) in the form of a clock and in a field using a CCD for example. The video data of frequency (fsh) is supplied as it is to the processor 1 and then delivered as it is. While the video data of frequency (fsl) is supplied to a terminal 2. A clock pulse CK1 synchronized with the frequency (fsl) is supplied to a terminal 4. A pulse CK1 is supplied to a clock and control signal producing circuit 5, and a clock pulse CK2 of frequency (fsh) is formed. A time axis converting circuit 6 consisting of an RAM for example is provided between the terminal 2 and the device 1. Thus an adversely converted video data is obtained at an output terminal 3.



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